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A New Method of APWM Resonant Inverter Topology for High Frequency AC Power Distribution Systems

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ABSTRACT

In this paper, an asymmetrical pulse-width-modulated (APWM) resonant inverter topology is presented for high frequency ac power distribution systems. The inverter system is comprised of simple power and control circuitry. The detailed analysis shows that the proposed inverter has very low total harmonic distortion, near-zero switching losses, and fast transient response. Open loop and Closed loop Simulation results are presented to prove the performance of the proposed inverter.

Key words: APWM, High frequency, Resonant Inverter, Harmonic distortion, PWM topology.

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I. INTRODUCTION

Present and future high-speed microprocessors are becoming highly dynamic power loads to their power supplies with the simultaneous increase in power demand and decrease in supply voltage level, new challenges arise to the power distribution and power supply design. Recently, a number of publications [1]–[4] have proposed high frequency ac (HFAC) power distribution system (PDS) as one of the alternative solution to powering the future telecommunication and computer systems. Generally, a HFAC distribution system uses a front-end inverter as "silver box" to generate high frequency ac voltage for distribution. Then this ac voltage is converted to the specific dc voltage level by a point-of-use ac/dc converter (also known as ac voltage regulator module ac VRM) to power the processors. Compared to the conventional dc PDS, two conversion steps (the rectification in the front-end inverter and the inversion in the VRM) are eliminated in the HFAC PDS. Therefore, HFAC PDS is expected to have higher performance in terms of efficiency, size, cost, and reliability.

The proposals for the ac bus of the HFAC PDS range from trapezoidal wave to sinusoidal wave with bus frequency in MHz. Generally, the sinusoidal ac bus is recognized to be the best for very low EMI and RFI. However, it is more difficult to design and implement. In this paper, an asymmetrical pulse-width-modulated (APWM) resonant inverter topology is proposed as the front-end inverter of HFAC PDS. The switching frequency is increased into the megahertz range to improve the power density and Performance of switched-mode converters, interest has been shifted from pulse width modulation (PWM) to current- programmed and resonant modes of operation. Pulse width modulation is used in a majority of converters [5] [7] switched below a few hundred kilohertz because of its simplicity. In a PWM converter, the output is controlled by varying the pulse width or duty ratio of the switching waveforms. A current loop can be put around a PWM topology as described in [6] to form a current-mode converter. Current-mode control is gaining popularity because it offers improved performances, such as fast response, inherent current protection, and ease of paralleling.

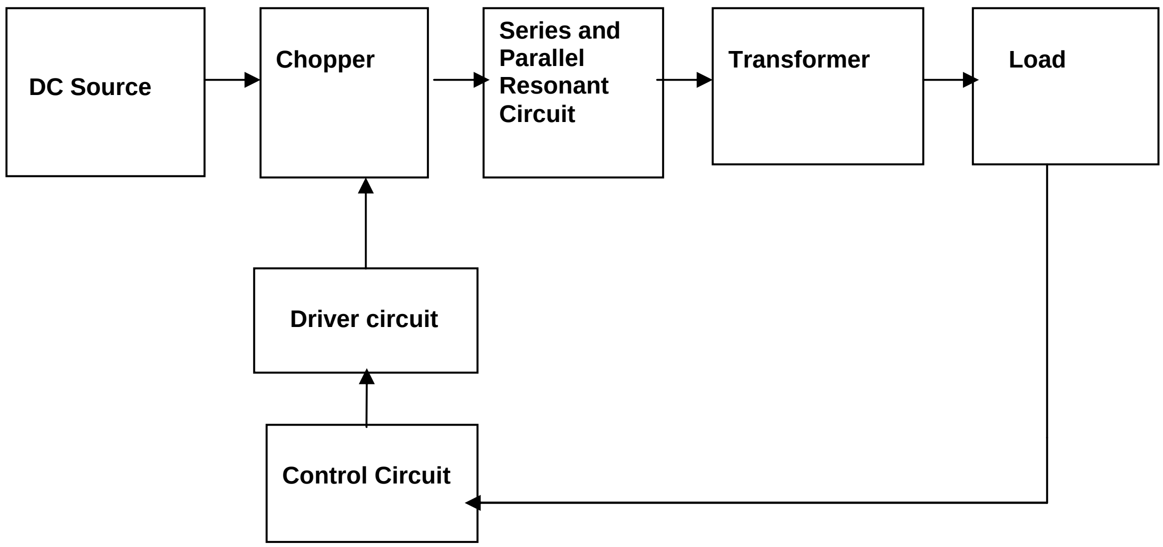

Fig.1. Block diagram of Proposed APWM resonant inverter topology

In a current-programmed converter, the output is controlled by a reference current, which is compared to a converter current to determine switching instants. Resonant conversion [8] is preferred to PWM or current-mode control in applications involving high power and high switching frequency. The switching loss in a resonant converter is low because the switching devices is turned on or off at practically zero voltage or current. The sensitivity to parasitic inductance or capacitance is reduced because these parasitic can be a part of the resonant circuit. In its most widely used configuration, a resonant converter is excited by a bipolar square wave, generated from a dc input by a half-bridge or full-bridge circuit.

The switching frequency is then varied to control the output voltage. Frequency control, however, causes many problems as the switching frequency has to be varied over a wide range to accommodate the worst combinations of load and line. For operation below resonance, filter components are large because they have to be designed for the lower frequency range. For operation above resonance, fast electronics are required to maintain control at the upper frequency range. Keeping the switching frequency constant and controlling it by pulse width modulation [5]are obvious ways to eliminate the problems associated with frequency variation. Another problem, found in a series resonant converter, is the loss of control at light load El]. Pulse width modulation solves this problem because as the time during which the source is connected to the converter is reduced to zero, so is the output voltage. This is because the power loss, which results from a constant circulating current at the input, is relatively independent of the line or load. Pulse width modulation or some current-controlled switching that reduces the amount of circulating current will improve the partial-load efficiency.

The resonant circuit has the following Functions:
a) It converts the unidirectional voltage into resonating series Current and parallel voltage.

b) It provides ZVS for the inverter switches.

c) It blocks dc component of the unidirectional voltage from Passing to the high-frequency transformer.

The proposed system having the following advantages

- Zero switching losses
- Fast transient response
- High efficiency
- Both the power and control circuits are simple

The circuit description, operating modes, and the control principle of the proposed inverter are given in Section II.. Finally, in Section III, simulation results are shown to prove the performance of the proposed inverter.

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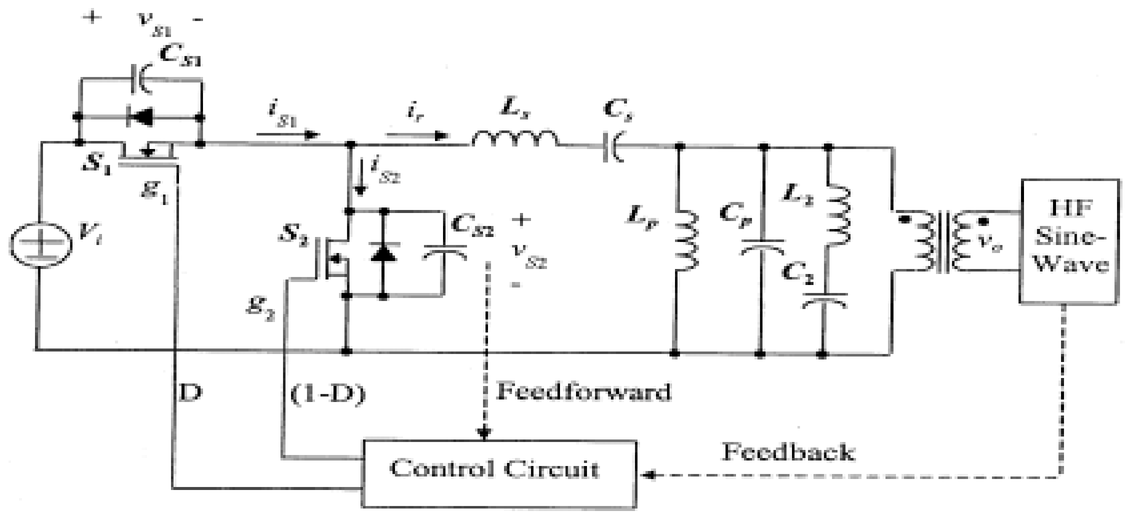

Fig.2 Proposed APWM resonant inverter topology

II. APWM RESONANT INVERTER TOPOLOGY

A. Circuit Description

Fig. 1 shows the block diagram of proposed system of resonant inverter topology and Fig.2 shows a circuit diagram of an APWM resonant inverter, which consists of a chopper, a series-parallel resonant circuit, a Second harmonic trap and a high-frequency transformer. The chopper converts input dc voltage into a high frequency unidirectional voltage at its output. The control circuits and driver circuits are used to generate the driving pulses. These driving pulses are used to make the chopper ON and Off. The resonant circuit consists of a series branch and a parallel branch. To achieve zero voltage Switching (ZVS) and maximum power transfer, the series resonant branch is tuned at the operating frequency, and the parallel Branch is off-tuned to provide inductive impedance at the operating frequency.

The resonant circuit has the following Functions:

a) It converts the unidirectional voltage into resonating series current and parallel voltage
b) It provides ZVS for the inverter switches.
c) It blocks dc component of the unidirectional voltage from passing to the high-frequency transformer.

The high-frequency transformer provides matching and isolation for the output of the inverter. The feed-forward and feedback control loops are employed to achieve fast transient response against the line and load variations.

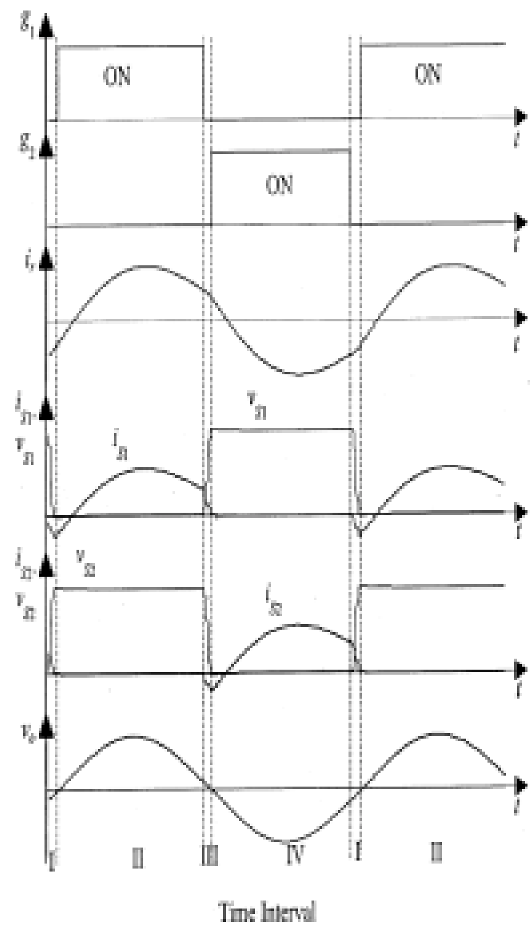

Fig.3 operating waveforms of the inverter.

B. Operating Principle

Fig. 3 shows key operating waveforms of the proposed inverter of Fig. 2. For each switching cycle, the inverter operates in the following four intervals.

Interval I:
At the beginning of this interval, switch s2 is turned off. Because of the negative resonant current, capacitor Cs1Starts to discharge into the resonant circuit. Once the Voltage across Cs1 reaches zero, the negative resonant current Forces the anti-parallel diode Ds1 to conduct.

Interval II:
At the beginning of this interval, switch S1 is turned on under zero voltage and a positive voltage Vi appears at the Output of the chopper. Power flows from dc input to the Resonant circuit and to the output load.

Interval III:
At the beginning of this interval, switch S1 is turned off. Because of the positive resonant current, capacitor Cs2 Starts to discharge. Once the voltage across capacitor Cs2 Reaches zero, the positive resonant current forces the anti parallel Diode Ds2 to conduct.

Interval IV:
At the beginning of interval IV, switch S2 is on under zero voltage and the output voltage of the chopper is clamped to zero. The energy stored in the resonant circuit during interval II now freewheels through switch S2 and Keeps supplying the power to the load.

The above description of the inverter operation reveals that:

i) Turn-on switching losses are zero since the anti-parallel diode always conducts prior to the switch.

ii) The drain-to-source losses are eliminated since the capacitor across the switch always discharges into the resonant circuit.

iii) Turn-off switching losses are much reduced due to the use of a large capacitor across the switch, which provides a slow rise of the voltage across the switch.

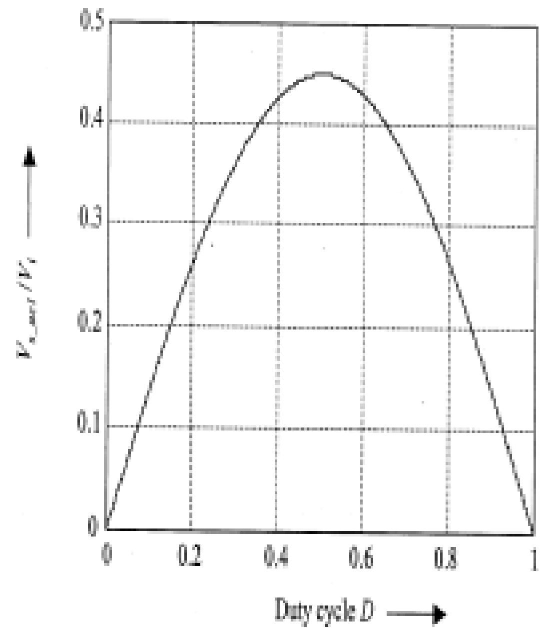

Fig.4 Output voltage control of the proposed

Control Principle

For APWM control technique [5], the complementary gating Signals with leading-edge delays are applied to switches S1 and S2. The voltage at the output of the chopper can be represented by the following Fourier series

$$v_{s2} = V_i \cdot D + \sum_{n=1}^{\infty} \frac{\sqrt{2}V_i\sqrt{1-\cos 2n\pi D}}{n\pi} \sin(n\omega_o t + \theta_n) \quad (1)$$

Where D is the duty cycle for switch S1, and

$$\theta_n = \tan^{-1}\left(\frac{\sin 2n\pi D}{1-\cos 2n\pi D}\right). \quad (2)$$

Because of the dc-block capacitor Cs and the series-parallel resonant circuit, only the ac fundamental component Vs2 of is considered to explain output voltage control

Fig.4 shows the RMS output voltage as a function of the duty cycle. This figure shows that the output voltage of the inverter can be controlled by changing the duty cycle either from 0 to 0.5 or from 0.5 to 1.0.

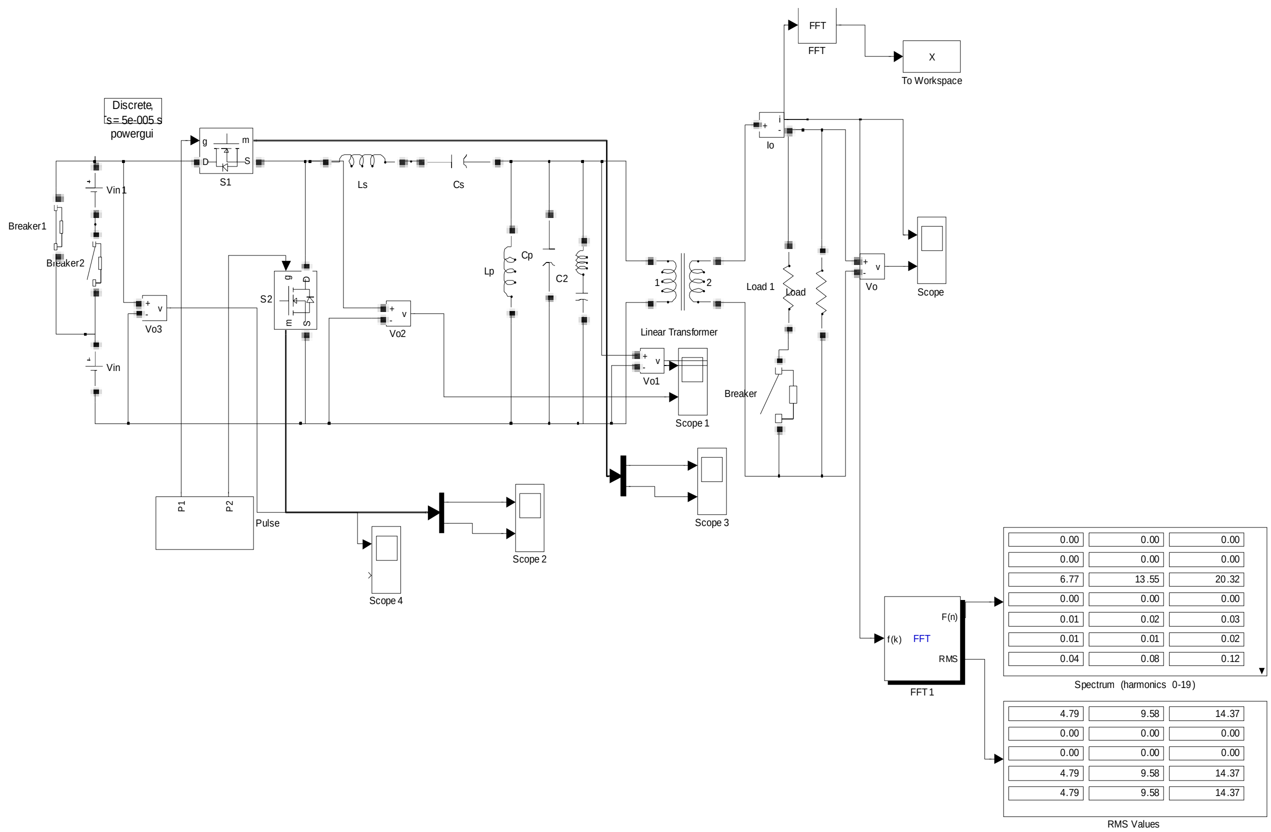

Fig.5.Open loop simulation circuit

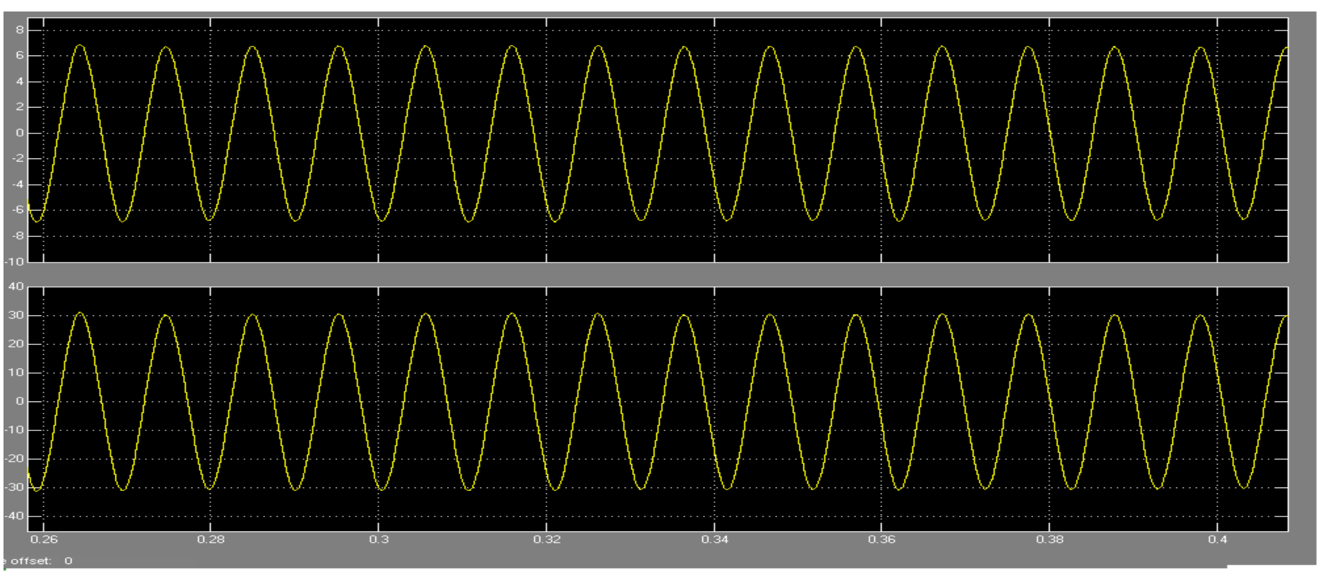

Fig.6.Open loop Output current and voltage waveforms

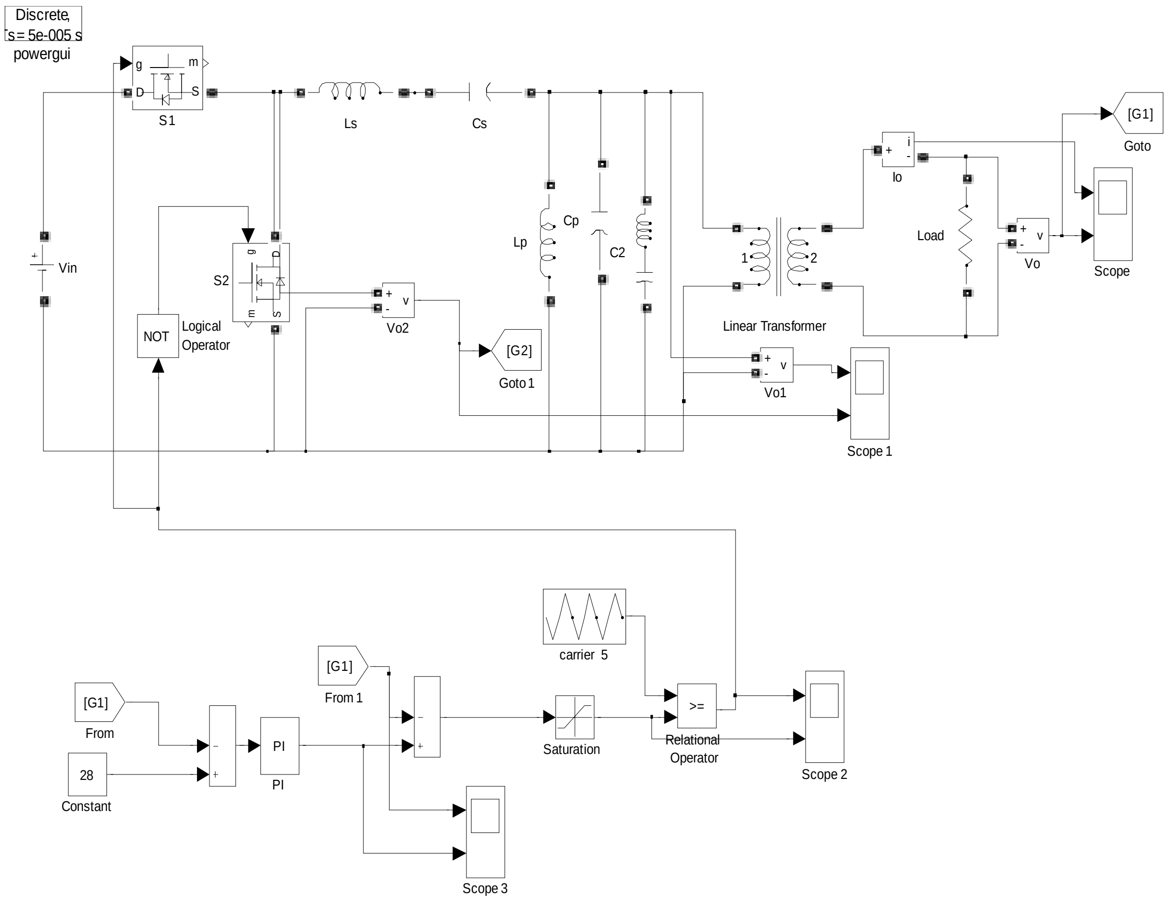

Fig.7. Closed simulation circuit

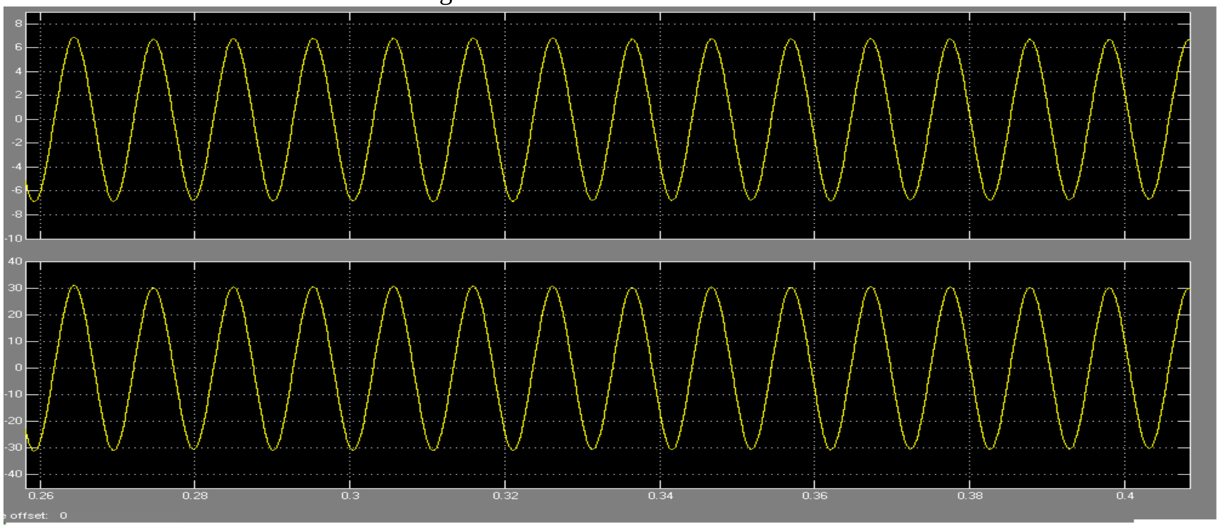

Fig.8.Closed loop Output current and voltage waveforms

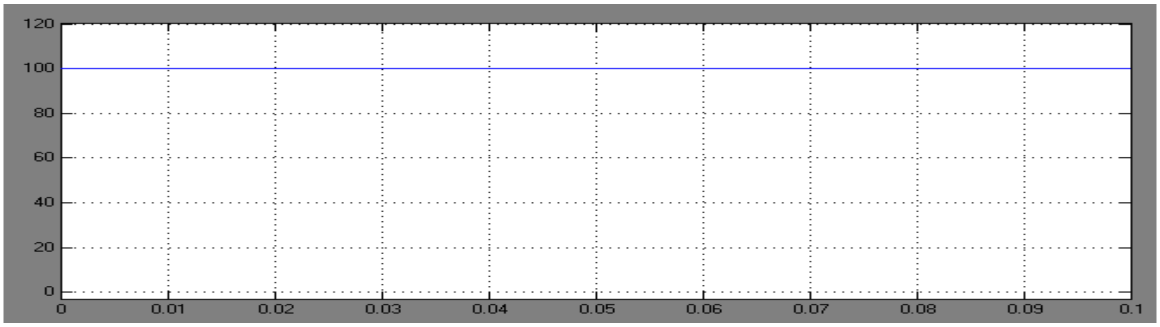

Fig.9.D.C input voltage

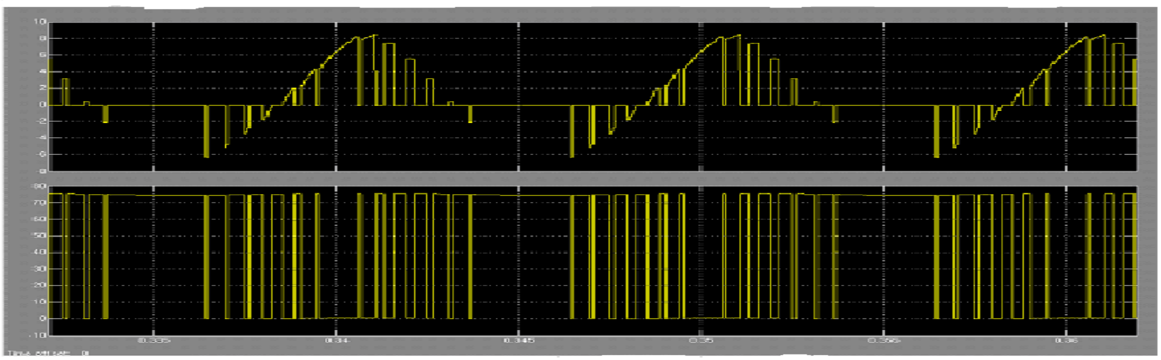

Fig.10. Asymmetrical pulse width modulation Waveform

III .SIMULATION RESULTS

The simulation results show that the proposed inverter generates near sinusoidal voltage waveform at the output, which has about 2% and 1.1% THD at rated load when the minimum (80 V) and maximum (110 V) input voltage is applied, respectively. Simulation results also show that ZVS is not lost at light load for the whole input voltage range. The simulation diagram of the open loop system and its output of current and voltage waveforms are shown in Fig. 5. & Fig. 6.The closed loop circuit model is shown in Fig.7.The output is sensed and it is compared with the reference voltage. The error is given to a PI controller, the output of PI controller adjusts the pulse width to bring the voltage to the set value. Fig.8.shows the closed loop inverter output of current and voltage waveforms. Fig.9.shows the DC input voltage, and Fig.10.shows the Asymmetrical pulse width modulation Waveform of the proposed inverter. The control loop uses the modulated integral control as a feed forward loop to provide pre-regulation for the feedback loop. A load voltage feedback loop is also included to compensate the resonant tanks of the inverter and the RC filter of the feedback rectifier. Simulation results show that the proposed inverter has fast transient response against the line and load variations.

IV. CONCLUSION

APWM resonant inverter has been presented and analyzed. The simulation results are in line with the predictions. This work deals with simulation studies .Hardware is not in the scope of this work. The simulation results are proved that the proposed topology has advantages like low switching losses and reduced stress. Also it providing near sinusoidal output voltage (THD less than 2% at the rated load). This sinusoidal voltage is used for induction heating .This system operates at high efficiency due to soft switching. Both the power and control circuits are simple, and have only two active switches. This topology is, therefore, an attractive candidate for the front-end inverter in HFAC distribution systems to power the future telecommunication and computer system.

References:

[1] J. Drobnik, "High frequency alternating current power distribution," in Proc. IEEE INTELEC'94, Vancouver, BC, Canada, 1994, pp. 292–296.

[2] J. Drobnik, L. Huang, P. Jain, and R. Steigerwald, "PC platform power distribution system: past application, today's challenge and future direction, in Proc. IEEE INTELEC'99, 1999.

[3] A. Gentchev and D. Arduini, "An AC high frequency quasi square wave buss voltage for the next generation of distributed power systems," inProc. HF Power Conv., Nov. 1998, pp. 89–103.

[4] P. Jain and H. Pinheiro, "A hybrid high frequency ac power distribution architecture for telecommunication systems," IEEE Trans. Power Electron., vol. 4, pp. 138–147, Jan. 1999.

[5] P. Jain, A. St-Martin, and G. Edwards, "Asymmetrical pulse-width-modulated resonant dc/dc converter topologies," IEEE Trans. Power Electron., vol. 11, pp. 413–422, May 1996.

[6] H. Jin, G. Goos, M. Pande, and P. D. Ziogas, "Feedforward techniques using voltage integral duty-cycle control," in Proc. IEEE PESC'92, 1992, pp. 370–377.

[7] R. L. Steigerwald, "A comparison of half-bridge resonant converter topologies," in IEEE Applied Power Electronics Conf., 1987 Proc.

[8] F. C. Schwarz, "An improved method of resonant current pulse modulation for power converters," in IEEE Power Electronics SpecialistsConf. 1975 Rec., pp. 194-204.

[9] A. F. Mikulski and R. W. Erickson, "Steady-state analysis of the series resonant converter," IEEE Trans. Aerosp. Electron. Syst., vol. AES-21, no. 6, pp. 791-799, Nov. 1985.

[10] F. G. Turnbull and R. E. Tompkins, "Design of a pulse width modulated resonant converter for a high output voltage power supply," in **IEEE Industry Applications Society Annu. Meet. I985 Rec.,** pp. 1145-**1150.** pp. 135-144.

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